Ferroelectric parallel-plate capacitors with copper electrodes for high-frequency applications

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Tunable capacitors with a $Cu/Pb_xSr_{1-x}TiO_3/Cu$ parallel-plate structure have been fabricated using a layer transfer method. The use of a Cu bottom electrode results in a giant electrode Q-factor $\times$ capacitor area product of $Q_{elec}A=3.79\times10^5$ μm^2 at 1 GHz. The dielectric constant at room temperature is 420 and the tunability amounts to 73% near a breakdown voltage of 35 V. The major advantages of the layer transfer method include low electrode losses, the freedom to select an auxiliary substrate and seed layer for ferroelectric film growth irrespective of their high-frequency properties, and the possibility to utilize a large variety of device substrates as they no longer act as template for film growth. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2825274]

Ferroelectric parallel-plate capacitors are under intense investigation for tunable device applications in microwave technology.[1,2] Perovskite materials such as $Ba_xSr_{1-x}TiO_3$ (BST) and $Pb_xSr_{1-x}TiO_3$ (PST) exhibit many desirable properties such as high tunability and relatively low dielectric loss. However, their integration with low-loss metallic electrodes has been problematic and this has hampered large-scale industrial applications. The main issues relate to the high deposition temperature (typically 600–800 °C) and reactive atmosphere that are required for the growth of crystalline ferroelectric films. These conditions limit the selection of the bottom electrode material, which in conventional parallel-plate capacitors also acts as seed layer for ferroelectric film growth. Currently, state-of-the-art bottom electrodes for high-frequency applications consist of a thick Pt layer or a combination of Pt and Au.[3,4] Unfortunately, the conductivity of Pt is relatively small (0.096×10^6 Ω^{-1} cm^{-1}), it is prone to oxygen diffusion, and tends to crystallize at elevated temperatures leading to pronounced roughness at the metal/oxide interface. All these effects contribute to electrode losses at gigahertz frequencies and hence limit the quality factor of ferroelectric capacitors. Moreover, Pt is not the ideal seed layer material for BST and PST film growth and, therefore, its use tends to compromise the structural quality of the ferroelectric film. Coplanar capacitors without bottom electrode are a viable alternative. However, this design requires much higher tuning voltages and exhibits lower dielectric tunability, which puts a constraint on many practical device applications.

In this letter, we report on a method for the fabrication of ferroelectric parallel-plate capacitors with low electrode losses. This method, which relies on the transfer of a ferroelectric film from an auxiliary to a device substrate, completely prevents the exposure of the bottom electrode to high temperatures and destructive reactive atmospheres. Here, the bottom electrode no longer serves as seed layer for ferroelectric film growth and therefore can be freely chosen. This enables the use of high-conductivity materials such as Ag (0.630×10^6 Ω^{-1} cm^{-1}) and Cu (0.596×10^6 Ω^{-1} cm^{-1}), which due to their thermal instability and corrosion properties are not commonly used in conventional parallel-plate capacitors. To demonstrate this method we use a ferroelectric $Pb_xSr_{1-x}TiO_3$ film with a nominal composition of $x=0.5$ and Cu electrodes.

The process steps for the fabrication of ferroelectric parallel-plate capacitors include (1) growth of a ferroelectric oxide on an auxiliary substrate, (2) deposition of a metallic bottom electrode *on top* of the ferroelectric film, (3) growth and planarization of a SiO_2 buffer layer, (4) transfer of the multilayer stack to another substrate, (5) removal of the auxiliary substrate by a combination of grinding and etching, and (6) deposition and patterning of a top electrode. In this study, we first deposited a 660 nm thick PST film using sol-gel onto a 100 mm silicon wafer with a 100 nm Pt/10 nm Ti/SiO_2 seed layer. Several spin coating/drying cycles of the precursor solution were conducted at room temperature (spin coating) and 200 °C (drying) and the resulting PST film was crystallized by annealing at 650 °C for 15 min. For adhesion purposes, we then first sputtered a thin TiW layer (10 nm) before depositing a 650 nm thick Cu bottom electrode and another TiW film (20 nm). Next, a 1000 nm thick SiO_2 was grown by plasma enhanced chemical vapor deposition and this was planarized by chemical-mechanical polishing. Layer transfer to a 100 mm quartz substrate was achieved by vacuum bonding at room temperature and the bond was subsequently strengthened by heating at 200 °C for 2 h in vacuum. The auxiliary silicon substrate was then thinned by grinding to <100 μm which then peeled off along the Pt/PST interface. Finally, a 650 nm thick Cu top electrode with a 20 nm TiW adhesion layer was sputtered and patterned by photolithography for electrical characterization. The process steps for the Cu/PST/Cu parallel-plate capacitors are sche-

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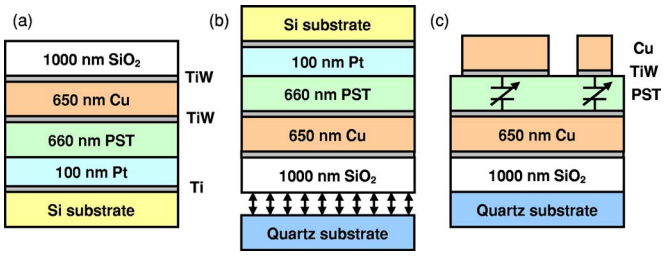

FIG. 1. (Color online) Schematic illustration of the fabrication of Cu/PST/Cu parallel-plate capacitors by layer transfer.

matically illustrated in Fig. 1. Dielectric measurements were performed with an Agilent-4294A precision impedance analyzer and a HP-8720D network analyzer. The capacitor test structures were connected to the analyzers by Cascade microprobes, whereby the signal leg contacted a well-defined small electrode and the ground leg a much larger area that efficiently coupled to the continuous bottom electrode. Standard tape tests on the final multilayer stack revealed good adhesion between the individual layers.

Figure 2(a) shows a bright-field transmission electron microscopy (TEM) image of the PST parallel-plate capacitor with Cu bottom and top electrodes. The PST film consists of several distinctive granular layers which are the result of multiple spin coating and drying steps during the sol-gel deposition process. The randomly distributed PST grains are polycrystalline, as illustrated by the θ-2θ x-ray diffraction scan of Fig. 2(b). The magnetron sputtered Cu layers, on the other hand, contain some misoriented grains with (111) and (100) out-of-plane texture and electron diffraction patterns (not shown) indicate the presence of twins, defects that are quite common in Cu. No clear epitaxial relationship between the PST film and the Cu electrodes does exist.

More detailed bright-field TEM images of the electrode/oxide interfaces are shown in Figs. 2(c) and 2(d). The Cu bottom electrode and the PST film are separated by a rough interlayer with dark contrast. This layer corresponds to TiW that, when grown on top of the relatively rough ferroelectric film, diffused into the PST grains. In contrast, the interface between the PST film and the Cu top electrode is sharp, as

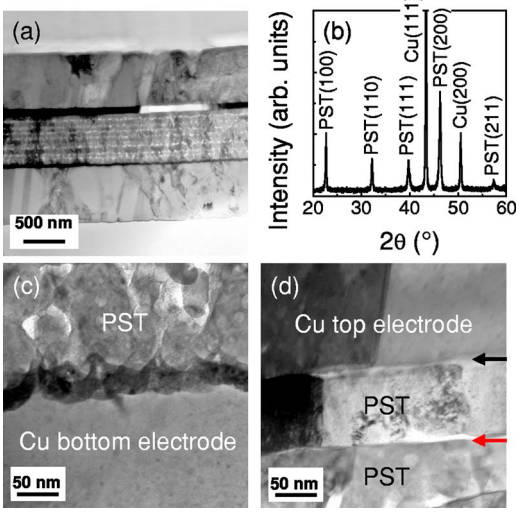

FIG. 2. (Color online) (a) Bright-field TEM image and (b) θ-2θ x-ray diffraction scan of the Cu/PST/Cu capacitor structure. (c) and (d) show bright-field TEM images of the Cu bottom electrode/PST layer and the PST layer/Cu top electrode interfaces, respectively.

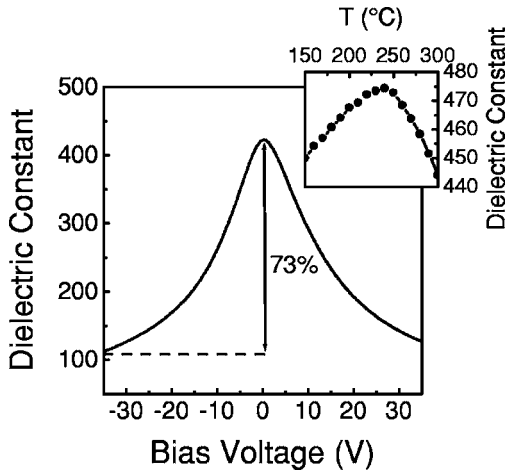

FIG. 3. Dielectric constant vs bias voltage curve at 1 MHz and room temperature indicating a dielectric tunability of 73% at 35 V. The inset shows the variation of the dielectric constant with temperature.

indicated by the upper arrow in Fig. 2(d). This clearly indicates that the original PST/Pt interface on the sacrificial substrate was smooth. Moreover, limited adhesion between Pt and PST films facilitated the complete removal of Pt after layer transfer. Finally, subsequent sputtering of the Cu top electrode on the exposed PST film did not introduce pronounced interface roughness. The lower arrow in Fig. 2(d) indicates a sharp interface between the PST layers that were formed during the first and second sol-gel spin-coating steps. The different layer morphology is due to dissimilarities between the films onto which these layers were spun, i.e., Pt and PST, respectively.

Figure 3 shows the bias dependence of the dielectric properties of a Cu/PST/Cu parallel-plate capacitor at a frequency of 1 MHz. The zero-bias dielectric constant at room temperature is 420 and the dielectric tunability ($[\varepsilon(0)-\varepsilon(V)]/\varepsilon(0)$) amounts to 73% at a typical breakdown voltage of 35 V, which compares well with other studies on polycrystalline PST parallel-plate and coplanar capacitors.[5,6] The dielectric constant increases with temperature and peaks at 240 °C where a ferroelectric-paraelectric phase transition occurs (see inset of Fig. 3). Hence, the PST film exhibits a spontaneous ferroelectric polarization at room temperature.

The PST film and Cu electrodes both contribute to the total dielectric loss of the Cu/PST/Cu parallel-plate capacitors. To a first approximation, the measured loss tangent ($\tan \delta_m$) can be written as

$$\tan \delta_m = \frac{1}{Q_m} = \frac{1}{Q_{\mathrm{PST}}} + \frac{1}{Q_{\mathrm{elec}}},$$

where Q represents the quality factor of the different components of the capacitor in a simple equivalent circuit. Since the electrode loss scales with the size of the capacitor, the quality factors of the PST film and electrodes can be determined separately by measuring the loss tangents as a function of capacitor area.[7] The experimental results at a frequency of 1 GHz are shown in Fig. 4. In this case, $\tan \delta_m = 1/Q_{\mathrm{PST}} + A/(Q_{\mathrm{elec}}A)$ and fitting the data give $Q_{\mathrm{PST}}=26$ and $Q_{\mathrm{elec}}A=3.79\times10^5$ μm^2. The quality factor of the electrodes is very large, which is mainly due to the use of high-conductivity Cu on both sides of the PST film. For a capacitor with a diameter of 10 μm, for example, it is nearly 5000

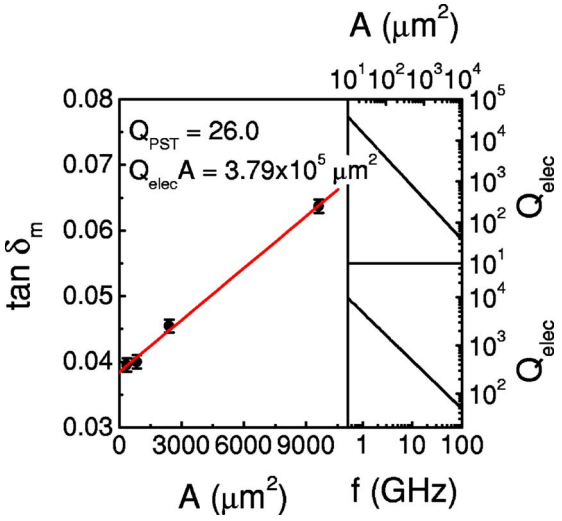

FIG. 4. (Color online) Measured dielectric loss (tan δ_m) as a function of Cu/PST/Cu capacitor area at 1 GHz. The upper right and lower right graphs show the variation of the electrode quality factor as a function of capacitor size (at 1 GHz) and frequency (for a capacitor with a diameter of 10 μm). These dependencies follow from the experimentally determined value of $Q_{elec}A = 3.79 \times 10^5$ μm^2.

at 1 GHz. Moreover, as $Q_{elec} \sim 1/f$, the quality factor of the electrodes is anticipated to remain larger than 100 up to a frequency of about 50 GHz (see lower right panel in Fig. 4). This clearly demonstrates the potential of the layer transfer method for the fabrication of ferroelectric parallel-plate capacitors with low-loss electrodes, which holds a great promise for microwave device applications. In addition, it enables measurements of true losses in ferroelectric films at high frequencies. The PST film in this study is in the ferroelectric phase at room temperature and, hence, piezoelectric transformations, domain wall movement, and scattering by spontaneous polarization do contribute to the dielectric loss.[8] Other possible sources of loss are the boundaries between the randomized PST grains and the metal/oxide interface layers.

Besides the obvious advantage of high-conductivity bottom and top electrodes, the layer transfer method also facilitates the use of microwave-compatible device substrates. Thick electrodes that are normally utilized to minimize substrate losses are therefore no longer a prerequisite for low-loss operation at high frequencies. In particular, silicon, a popular substrate choice for conventional parallel-plate capacitors, will contribute to dielectric losses if the electrode thickness is smaller than the electromagnetic penetration length or so-called skin depth. For Pt and Cu electrodes, for example, the skin depths at a frequency of 1 GHz are about 5 and 2 μm, respectively. By transferring the ferroelectric film onto a microwave-compatible substrate such as quartz, the substrate losses are small even for relatively thin metallic electrodes.

Finally, the auxiliary substrate and seed layers can be chosen such that their thermal expansion characteristics mimic those of the ferroelectric film. This limits the formation of cracks and the buildup of thermal strain after high-temperature film growth, features that tend to reduce the performance of parallel-plate capacitors.[9] As the auxiliary substrate and seed layers are removed after layer transfer, their selection is not compromised by their high-frequency properties.

In summary, we have demonstrated that a layer transfer method can be used for the fabrication of ferroelectric parallel-plate capacitors. By decoupling the function of seed layer and electrode, it was possible to use Cu as the bottom electrode and this resulted in very small electrode losses in Cu/PST/Cu capacitors at gigahertz frequencies. Besides, as the substrate and seed layer for ferroelectric film deposition do no longer have to be microwave compatible (they are removed after layer transfer), this method allows for a variety of seed layer architectures that will promote high-quality oxide growth. With the drastic reduction of electrode losses and the opportunity for improved ferroelectric film growth, the layer transfer method holds a great potential for tunable device applications in microwave technology. Moreover, it enables fundamental studies on intrinsic loss mechanisms in ferroelectric films at gigahertz frequencies as these are no longer blurred by losses in the electrodes and substrate.

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[1] A. K. Tagantsev, V. O. Sherman, K. F. Astafiev, J. Venkatesh, and N. Setter, J. Electroceram. **11**, 5 (2003).
[2] N. Setter, D. Damjanovic, L. Eng, G. Fox, S. Gevorgian, S. Hong, A. Kingon, H. Kohlstedt, N. Y. Park, G. B. Stephenson, I. Stolitchnov, A. K. Taganstev, D. V. Taylor, T. Yamada, and S. Streiffer, J. Appl. Phys. **100**, 051606 (2006).
[3] B. Acikel, T. R. Taylor, P. J. Hansen, J. S. Speck, and R. A. York, IEEE Microw. Wirel. Compon. Lett. **12**, 237 (2002).
[4] A. Vorobiev, P. Rundqvist, K. Khamchane, and S. Gevorgian, Appl. Phys. Lett. **83**, 3144 (2003).
[5] H. Xu, M. Shen, L. Fang, D. Yao, and Z. Gan, Thin Solid Films **493**, 197 (2005).
[6] K.-T. Kim and C.-I. Kim, Thin Solid Films **420/421**, 544 (2002).
[7] D. C. Dube, J. Baborowski, P. Muralt, and N. Setter, Appl. Phys. Lett. **74**, 3546 (1999).
[8] O. G. Vendik, E. K. Hollman, A. B. Kozyrev, and A. M. Prudman, J. Supercond. **12**, 325 (1999).
[9] T. R. Taylor, P. J. Hansen, B. Acikel, N. Pervez, R. A. York, and S. K. Streiffer, Appl. Phys. Lett. **80**, 1978 (2002).